

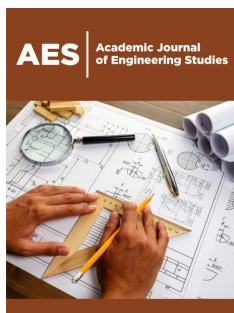
New Packaging for Efficient Heat Dissipation of Microchannels based on TSV Technology

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Abstract

The new microchannel packaging for efficient heat dissipation based on the three-dimensional stacking structure requires the combination of silicon-based interposer plates and microchannel technology. The research in this field should not only focus on the heat dissipation application of microchannels. In the future, it should consider taking into account the transmission of electrical performance, further expand the application, and achieve higher three-dimensional system integration goals. Taking the integration of the new microchannel heat dissipation structure - Through Silicon Via (TSV) as the research object, systematically study the integrated structure design of the microchannel, the new integrated process path, the packaging path of the highly reliable microchannel structure, and establish the corresponding heat dissipation model, and then verify the process architecture from the aspects of simulation and actual measurement. The research on the new packaging of microchannel efficient heat dissipation based on interposer plate technology has practical significance and value for the current miniaturization and reconfigurable development of electronic equipment.

Keywords: Microchannel; Through Silicon Via (TSV); Heat dissipation; Advanced microsystem integrated packaging

Introduction

The radio frequency electronic equipment is developing towards high integration and high power, which strongly drives the progress of radio frequency microsystem technology. The core technology of the current mainstream 2.5D/3D advanced microsystem integrated packaging system is three-dimensional integration, and the packaging is developing towards three-dimensional integration. With the gradual application of three-dimensional integrated microsystem technology, the density of functional modules and high-power chips integrated in the system increases rapidly, and the required heat dissipation density and difficulty increase sharply. It is specifically reflected in three aspects: high surface heat flux, high volume heat flux density and thermal stacking. When the power density of the microsystem exceeds 100 W/cm², the traditional cooling methods such as heat sinks, fan cooling and heat pipes can no longer meet its heat dissipation requirements. The heat dissipation problem has become one of the key bottlenecks restricting the development of microsystem integration of high-power electronic systems. The power density of advanced electronic modules in equipment fields such as radio frequency microsystems, high-performance computing and high-power lasers has exceeded 500 W/cm², posing severe challenges to heat dissipation technology. Preparing embedded microfluids in electronic modules (chips, interposer boards or cold plates) through micro-nano processing technology to obtain efficient liquid cooling heat dissipation is an important technical method to break through the "Thermal bottleneck" of electronic modules at present, and the microchannel heat dissipation technology is the preferred means that takes into account both heat dissipation and integration requirements [1-5].

The Current Situation and Bottlenecks of Microchannel Heat Dissipation Technology

Microchannel heat dissipation

As an active heat dissipation technology, microchannel has extremely low thermal resistance, large heat transfer coefficient and good heat dissipation efficiency. The previous research work has on the one hand preliminarily proved the feasibility and advancement of the integrated microchannel heat dissipation technology for the heat dissipation problem of high-power chips, and some technologies have gradually entered the stage of engineering application research [5-10]; but on the other hand, it can be seen that the realization progress of microchannel heat dissipation technology and three-dimensional integration is relatively slow. The three-dimensional integrated microchannel heat dissipation technology still faces huge challenges of complex problems such as compatible manufacturing and reliability impact, and there is still a long way to go before mature application.

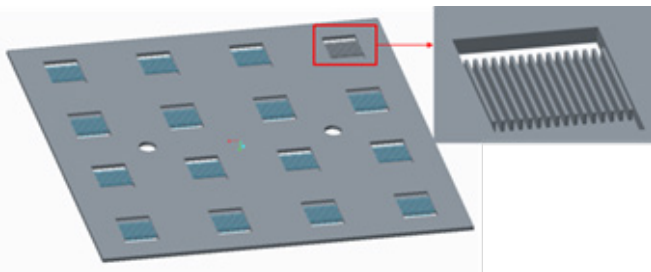


Figure 1: The basic structure of Microchannels.

It mainly faces challenges in materials, structures, processes and applications, and the industry has carried out a large amount of research in many aspects. For 3D stacking, IBM adopts a double-sided microchannel liquid cooling solution. The top surface adopts a manifold microchannel liquid cooling plate, and the bottom adopts a TSV interposer plate with embedded microchannels. DARPA has also released the ICE-COOL program (Intrachip Enhanced Cooling Program) and proposed a solution of embedding microchannels between or within the chips to solve the cooling of 3D stacking [11-13]. In addition, Georgia Tech uses embedded micro-turbulence columns within the chip and a soldering ring connection process between the chips to achieve 3D intra-chip liquid cooling. 3D intra-chip liquid cooling mainly needs to solve the problems of inter-chip connection and intra-chip channel sealing.

At present, microchannels can be fabricated using a variety of materials, including ceramics, metals, glass, silicon, etc. Silicon-based microchannel packaging can be compatible with semiconductor and MEMS processes [14,15], has better integration, and silicon is also an excellent conductor of heat. However, in terms of the reliability research of silicon-based microchannel packaging and the related research on the compatibility packaging design based on three-dimensional integration, it still remains at the experimental sample and theoretical research stage. Effective structural stress solutions and three-dimensional interconnection solutions have not yet been formed. It is necessary to accommodate the heat dissipation

at the device end, and at the same time, match the thermal stress of the microchannel with the rear support structure, and the inlet and outlet water structure. On the other hand, while meeting the heat dissipation requirements, the compatibility scheme of vertical interconnection transmission of signals also needs further study.

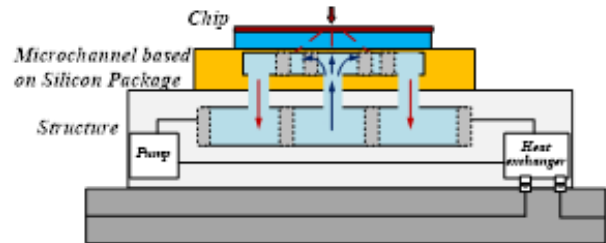


Figure 2: Conventional integration architecture of micro-channel [15].

The challenges

The efficient heat dissipation of new microchannel packaging based on the three-dimensional stacking structure requires the combination of silicon-based interposer plates and microchannel technology. Silicon interposer plate technology is a packaging substrate structure based on silicon-based MEMS processing technology to achieve vertical signal transmission. The integration of microchannels and interposer plates depends on silicon-based materials.

The uniqueness of silicon materials lies in that

- (1) It has excellent process compatibility and can be integrated and manufactured on a common silicon-based MEMS process platform;
- (2) The thermal conductivity of the substrate material reaches $150\text{W}/(\text{m}\cdot\text{k})$;
- (3) The thermal expansion coefficient has good matching with the device, and thermal matching with various materials such as silicon, gallium nitride, and gallium arsenide can be achieved;
- (4) Vertical interconnection structures and horizontal wiring can be integrated on the surface of silicon-based materials to complete the packaging of device circuits.

However, there are also application problems, including

- (1) The material is hard and brittle and cannot directly withstand environmental impacts such as impact and vibration, and needs to be transferred to the next-level packaging structure;
- (2) There is a large thermal mismatch with the rear structure and the substrate, and the problem of thermal stress matching needs to be emphasized.

From the existing reports of microchannels, in some literatures, only focusing on the heat dissipation application of microchannels, it is used as an independent heat sink and attached to the

proximal end of the heat source by gluing or welding. The further expansion application of electrical performance transmission is not considered, nor is it well compatible with three-dimensional packaging integration, only achieving miniaturization to replace the application of large heat dissipation fins; in some literatures, although the compatibility evaluation and research of microchannels and interposer plate technology have been carried out [16], the thermal stress matching of this packaging structure with the rear structure is not considered. In addition, in this part of the literature, TSV is integrated after the microchannel is fabricated first, that is, the vertical interconnection of the TSV interposer plate implemented by the via-last process limits the vertical interconnection density and cannot fully utilize the RDL layout inside the multi-layer silicon of the microchannel, failing to achieve effective utilization of the silicon layer of the microchannel; while our research group has been committed to the three-dimensional integrated packaging of TSV interposer plates and the compatibility research of microchannels in three-dimensional integration.

Based on the originally constructed TSV interposer plate technology and microchannel technology path, this project will take the multi-layer TSV interposer plate as the base layer and take the integration of the new microchannel heat dissipation structure - TSV interposer plate as the research object. Systematically study the integrated structure design of the microchannel, the new integrated process path, the packaging path of the highly reliable microchannel structure, and establish the corresponding heat dissipation model, and then verify the process architecture from the aspects of simulation and actual measurement. This new packaging research of microchannel efficient heat dissipation based on interposer plate technology has practical significance and value for the current miniaturization and reconfigurable development of electronic equipment.

Research On Thermal Design of Embedded Microchannel Structure

Construction of an integrated simulation model of TSV Interposer plate - Microchannel

Due to the complex structure of the microchannel system embedded and integrated based on interposer plate technology, and the large number of integrated channel substrates and the various types of channel structures [17-19]. Different channel structures, the proportion of channel area and the proportion of vertical interconnection area will affect the final heat dissipation effect [20-21]. The electrical connection and signal transmission of the interposer plate are all through electrical TSVs, which have a competitive relationship with the microchannels in the wiring space. The electrical performance of TSVs and the heat dissipation capacity of microchannels interact with each other. Therefore, it is necessary to conduct consistent design research on electrical TSVs and microchannels.

The design of equivalent thermal conductivity of the interposer based on hollow TSV

A layer of TSV interposer plate is interposed between the microchannel and the chip due to the electrical packaging

requirements. The presence of TSV leads to the thermal conductivity of the silicon interposer plate being different from that of pure silicon material, thus affecting the heat dissipation effect of the chip, and an optimized design study is required.

At present, there are generally three methods for calculating the equivalent thermal conductivity of the TSV interposer plate:

- a. Theoretical formula derivation;
- b. Simulation calculation, and then obtaining the empirical formula through fitting after obtaining the simulation data;
- c. Experimental method, obtaining the data through experiments and substituting it into the formula for calculation.

Integrated Embedded Thermal Design of TSV of the Channel Layer Interposer Plate and Microchannel

There is a competitive relationship between the microchannel and the electrical TSV in the wiring space. The larger the space occupied by the microchannel, the better the heat dissipation capacity, but it affects the layout of the electrical TSV, thereby affecting the electrical performance of the chip. Therefore, it is necessary to conduct a consistent design of the microchannel and the electrical TSV. The integration degree of the radio frequency microsystem is continuously improving. In high-performance and multi-functional radio frequency front-end modules, there are a large number of signal interconnection requirements such as radio frequency, control, and power supply, and the number of required electrical TSVs is continuously increasing. Therefore, when designing the distribution and geometric structure of the microchannel, it is necessary to ensure at the same time that there is enough space for the layout of the electrical TSV.

Based on the geometric structure of the microchannel, the number of TSVs fabricated on the microchannel wall can be calculated. Through model simulation design, the number of TSVs that can be accommodated under different heat dissipation capabilities can be obtained. The research results can adaptively select the heat dissipation layout scheme according to the requirements of system integration and heat dissipation.

Conclusion

The core idea of the new high-reliable integrated packaging technology path of microchannels originates from the demand pull of long-term three-dimensional integrated packaging applications and the inspiration of actual radio frequency system product projects. It has gradually emerged on the basis of a large amount of research work and has a relatively complete theoretical basis and experimental accumulation.

In the establishment of the simulation model of TSV interposer plate and microchannel, when cascading the established model, the thermal design model still needs to be further optimized. It is necessary to combine the simulation models of heat and mechanical stress, etc. The existing model is based on the traditional microchannel structure and needs to add structural features. Subsequently, through the analogy and optimization of the existing

model, the microchannel packaging simulation suitable for the new packaging structure will be determined, and optimized and iterated in combination with the physical test results.

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