

Fabrication of Single Crystal Silicon Nanomembranes



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Abstract

Silicon nanomembranes are thin, free standing sheets of single or poly-crystalline silicon, typically less than a micrometer thick, with lateral dimensions exceeding the thickness by several orders of magnitude. Nanomembranes have applications in flexible electronics, pressure sensing, photonic and phononic devices, sample mounts for microscopy, windows and beam splitters for optical and x-ray scattering measurements, and as a model system to perform fundamental investigations of nanoscale phenomena. This review covers fabrication processes for creating single crystal nanomembranes from a silicon-on-insulator (SOI) wafer as the starting material.

Introduction

Freestanding nanomembranes provide an ideal system for advancing nanoscience as well as for developing nanotechnologies. In addition to the advantages that crystalline silicon brings as an inexpensive semiconductor material with extremely well understood electronic and thermal properties and established processing methods, single crystal silicon membranes are

particularly useful due to their superior mechanical properties: they are strong, flexible, stretchable, bondable and highly resistant to thermal and mechanical fatigue. The primary methods for fabricating single crystal nanomembranes use silicon-on-insulator (SOI) wafer as the base material, which also makes such devices easily compatible with SOI-based microelectronics.

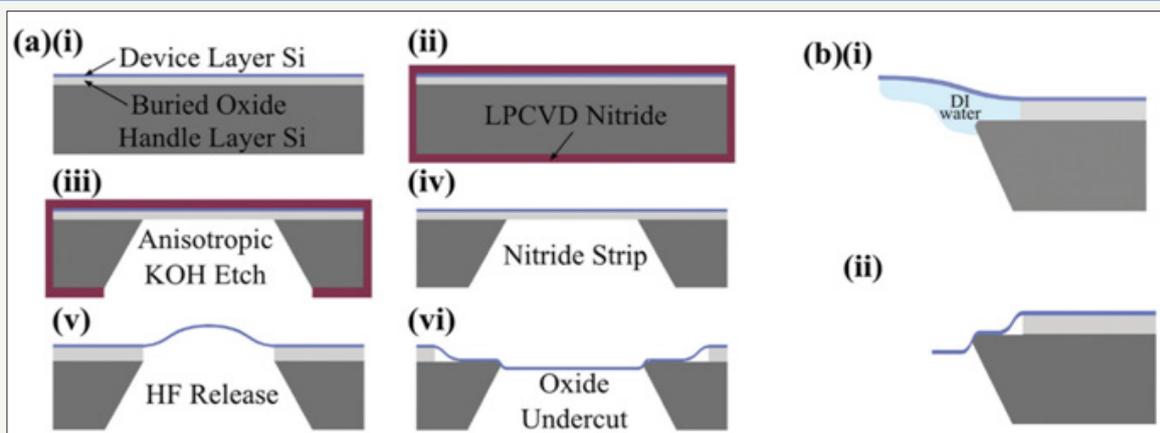


Figure 1: From [12] (a) Fabrication steps for producing nanomembranes from SOI. Parts (i) - (v) depict traditionally used silicon processing steps that typically result in buckled nanomembranes. Part (vi) is a modification to the process that flattens the membrane. (b) The mechanism for membrane flattening relies on the interfacial energy between silicon and water.

A primary hurdle in the fabrication of thin, flat nanomembranes arises from built-in compressive strains in the device layer of the SOI wafer. The fabrication process generally involves lithographic patterning and selective etching through the handle and buried oxide (BOX) layers of the SOI wafer, converting a selected region

of the device layer into a freestanding membrane supported only along its edges (Figure 1). This process results in buckled nanomembranes due to the removal of the underlying support structure holding the compressively strained device layer in place [1-5]. The extent of buckling can be large enough to restrict the

usefulness of the membrane structure, especially in microelectronic and micromechanical applications. Several approaches have therefore been used to mitigate this buckling and produce flat nanomembranes.

Discussion

One class of approaches is to completely release the membrane from the parent SOI and transfer it to a second frame. This can be done, for instance, by etching the BOX layer under the device layer through a series of etch holes and floating off the resulting membrane [6]. Another method involves a thermal expansion to compensate for the compressive device layer strains, followed by a direct wafer bonding step to transfer the device layer to a second substrate [7]. These techniques are particularly useful if a framing substrate other than the parent SOI wafer is desired.

On the other hand, several applications, especially those involving microelectronics and sensing have no need for a different framing substrate, or in fact, prefer the membrane to remain in its original SOI frame. A second class of approaches retains the membrane on the SOI wafer it was fabricated from, but uses one of several methods to flatten the membrane by compensating for the compressive strain in the device layer. For instance, significant flattening of the membranes can be achieved by patterning the

device layer to create strain relief structures that accommodate the majority of the compressive strain, leaving the suspended membrane region relatively flat [1,8,9]. A more controlled approach that puts the membrane in tension uses a silicon nitride over layer to frame the edges of the membrane and introduce a tensile strain that overcomes the inherent compressive strain in the device layer [10,11].

An alternative approach to creating flat nanomembranes in the parent SOI embraces the phenomenon of stiction, which is painstakingly avoided in traditional MEMS fabrication. In this process, the interfacial energy between silicon and water is used to put the membrane in a meta-stable tensile state [12]. Buckling amplitudes on the order of several micrometers are replaced by flat membranes with thicknesses as low as 5nm and out of plane deviations no larger than 10nm over a region spanning more than 100 μ m across. These flat membranes can be subsequently stabilized by a directed UV exposure followed by a thermal anneal, which bonds the membrane more strongly to the underlying silicon ledges and relieves some of the tensile strain and strain in homogeneity in the membranes. Membrane tension is monitored through a series of pressure tests, whose results are compared with finite element models (FEM) of the membrane deflection under uniform pressure loading (Figure 2).

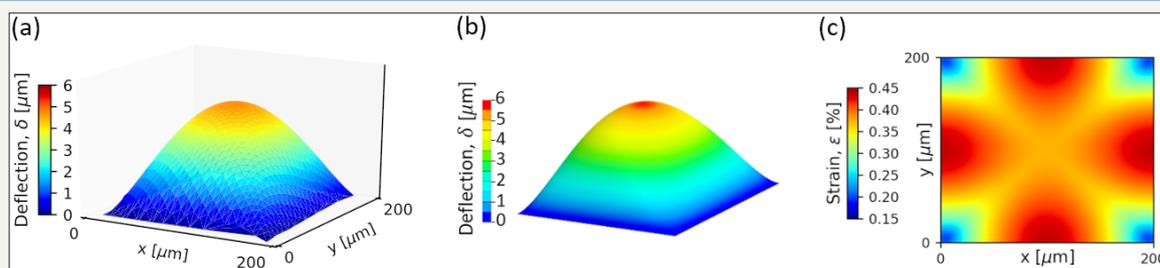


Figure 2: (a) Deflection of a 100nm thick membrane at a pressure of 20psi, measured by white light interferometry. (b) FEM solution of the same membrane under the same conditions. (c) Membrane strain map from the FEM analysis.

Note: Displacements in the z-direction are exaggerated to display the membrane shape.

Conclusion

Several processes have been developed for the fabrication of thin, flexible single crystal silicon nanomembranes. These membranes serve as model systems to investigate nanoscale size effects on electronic transport [13,14], phonon dispersions [15-19] and heat transfer [20,21]. Further modification of the membranes by lithographic patterning [22] or strain engineering [23] leads to additional functionalities such as photonic devices and flexible electronics. Recent work has extended the use of these techniques to other materials, such as germanium, silicon-germanium multilayers, and silicon-silicon dioxide hetero-structures [24-26] further expanding the scope of potential applications.

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